IN THE SPECIFICATION:

(A) On page 1, before the "BACKGROUND OF THE INVENTION" section, please add the following new section:

--RELATED APPLICATION DATA

This application is a divisional of U.S. Patent Appln. No. 09/404,920, filed on September 24, 1999, in the names of Frederic Reblewski, Olivier LePape, and Jean Barbier. This present application is entirely incorporated herein by reference.--.

is now a U.S. Patent 6,947,882

(B) Please amend the paragraph at page 10, lines 8-13 as follows:

Preferably, FPGA **100** also includes memory **112**, context bus **106**, scan register **108**, and trigger circuitry **110**. Memory **112** facilitates usage of FPGA **100** to emulate circuit designs with memory elements. Context bus **106**, scan register **108** and trigger circuitry **110** provide on-chip integrated debugging facility for FPGA **100**. These elements are described in U.S. ~~patent application serial number~~ Patent Appln. No. 08/542,838, entitled "A Field Programmable Gate Array with Integrated Debugging Facilities," ; which is hereby fully incorporated by reference.

(C) Please amend the paragraph at page 15, lines 14-19 as follows:

In an alternate embodiment of the present invention, signals are routed directly from I/O pins ~~510~~ 518 of FPGA **501** to/from I/O pins **533** of FPGA **503** without being routed through RC **502**. I/O circuitry **515** and **536** are both clocked by one of either signal routing clock **509** or signal routing clock **510**. Thus, even though a routing chip is not used in this alternate embodiment, the signal routing between FPGAs is still clocked by a signal independent of the user clock signal(s).